This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Previously presented) A method for fabricating an RF semiconductor device comprising:

forming a trench to define an active region and an element isolation region in a semiconductor substrate;

forming a plurality of gate lines within the active region of the semiconductor substrate, the plurality of gate lines not extending over a center of the trench;

forming an insulating layer on the plurality of gate lines and the semiconductor substrate;

forming at least one contact hole in the insulating layer within the active region without forming a contact hole within the element isolation region;

forming a contact plug in the contact hole; and

forming a conductive pattern layer that is electrically connected with the contact plug.

2. (Currently presented) A method as defined in claim 1, wherein the ~~plurality of~~ gate lines in the plurality are not connected with each other in the element isolation region.

3. (Previously presented) A method as defined in claim 1, wherein at least two of the plurality of gate lines are connected in the active region.

4. (Original) A method as defined in claim 1, wherein a thickness of the insulating layer is about 1000 to about 20000 angstroms.

5. (Original) A method as defined in claim 1, wherein a thickness of the conductive pattern layer is above 10000 angstroms.

6. (Previously presented) A method as defined in claim 1, wherein the insulating layer is one of an oxide and a polyimide.

7. (Previously presented) A method as defined in claim 1, wherein the plurality of gate lines are formed in order to minimize parasitic capacitance between the plurality of gate lines and the substrate.

8. (Previously presented) A method as defined in claim 1, wherein the plurality of gate lines are formed in order to minimize resistance of the plurality of gate lines.

9. (Previously presented) A method as defined in claim 1, further comprising metal contacts linking at least two of the plurality of gate lines.

10. (Previously presented) A method as defined in claim 1, wherein the plurality of gate lines do not extend along a longitudinal axis of the trench.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)